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KENYON & KENYON
1500 K STREET, N.W., SUITE 700
WASHINGTON, DC 20005

EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,807	JOURDAN, STEPHAN J.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/12/02, 11/13/01, and 10/24/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/12/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been examined.

Papers Received

2. Receipt is acknowledged of Information Disclosure Statement, Declaration, and Preliminary Amendment papers submitted, where the papers have been placed of record in the file.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 210.1, 210.2, 210.3, 201.N, and 1100. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to because the reference characters in figure 4 are described in the specification as being for figure 3 and the reference characters in figure 3 are described in the specification as being for figure 4. Corrected drawing sheets are

required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 22-24 are objected to because of the following informalities: the term "STD uop" is used but the term is not defined in the claims and the examiner is unfamiliar with this term. The examiner is taking the term to mean a microinstruction that indicates data to be written to memory for a store instruction as described by the background of the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 10-12, 15, 16, and 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 10 and 18 recite the limitation "the first microinstruction" in the second line of the claim. There is insufficient antecedent basis for this limitation in the claim. The claim is also written in poor grammatical fashion and difficult to understand. The examiner is taking the claim to mean, "In regard to claim 10 (18), Keller discloses the scheduling method of claim 5 (14), wherein the store microinstruction is one of a plurality of microinstructions representing a store instruction, wherein a first microinstruction is to transfer data to a store unit and a second microinstruction is to calculate an address of the store instruction," as disclosed by the specification.

9. Claim 15 recites the limitation "the marker." There is insufficient antecedent basis for this limitation in the claim. The examiner taking the claim to mean "the dependency pointer" as this is the terminology used in the parent claim as opposed to the marker terminology used in claim 5.

10. Claim 19 recites the limitation "the marker." There is insufficient antecedent basis for this limitation in the claim. The examiner taking the claim to mean "the dependency pointer" as this is the terminology used in the parent claim as opposed to the marker terminology used in claim 5.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 1-9, 13-17, and 21-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Keller (6,622,237).

13. In regard to claim 1, Keller discloses a scheduler (figure 1, element 36), comprising a plurality of scheduler entries (figure 3, element 66 and column 1, lines 11-13), wherein entries that store a load microinstruction include a first field for storage of microinstruction type data (figure 3, element 66, Type) and an administrative field having at least one field to store address operand pointers and an additional field to store a dependency pointer (figure 3, element 66, T). Column 11, lines 9-44 show that the "Type" field indicates the type of instruction, including a load type. This section also shows that the T field indicates or points out a load as being dependent on an older store and thus is a dependency pointer. Finally, the section shows that information such as operand register numbers (PR#s, an address pointer to a register operand) is also included in the entry. Since both the operand pointers and dependency pointers are stored in the entry, this makes up an administrative field. Figure 1, element 28 shows a microcode unit and thus the processor actually executes and schedules microcode instructions or microinstructions.

14. In regard to claim 2, Keller discloses the scheduler of claim 1, wherein the entries that store load microinstructions further comprise a field to store a valid bit associated

with the dependency pointer. Figure 3, element 66 shows a field "V" for valid, in each entry. This field is associated with the dependency pointer since it is in the same entry and providing information to the same instruction.

15. In regard to claim 3, Keller discloses the scheduler of claim 2, wherein a predetermined state of the valid bit in one of the entries indicates that scheduling of the load microinstruction in the one entry is to be deferred. The disclosure of Keller discloses the presence of a valid (V) bit in each scheduler entry for indicating validity of an entry holding a load as shown above. Column 14, line 50 – column 15, line 39 show that valid bits, such as that in the scheduler, are used throughout the system to indicate whether a dependency is valid. If a dependency is valid (valid bit set to a predetermined value) between a load and an older store, then as shown above the load is deferred.

16. In regard to claim 4, Keller discloses the scheduler of claim 1, wherein the presence of data in the dependency pointer in one of the entries indicates that scheduling of the load microinstruction in the one entry is to be deferred. Column 12, lines 43-46 state that by indicating the dependency of a load upon a store (using the T bit) scheduling of the load is inhibited or deferred until after the store is scheduled.

17. In regard to claim 5, Keller discloses a scheduling method for a load microinstruction, comprising:

a. predicting a collision between a new load microinstruction and an older store microinstruction; Column 10, lines 35 – 55 show that a STLF (store to load forwarding, column 2, lines 14-27) predictor makes a prediction for each load

instruction (new load) based on past executions whether it will interfere or collide with a store operation. Column 10, line 61 – column 11, line 8 shows that the embodiment of focus in the disclosure is where the store is older than the load.

b. when a collision is detected, determining whether data for the older store microinstruction is available;

c. if data for the older store is not available, storing the load microinstruction in a scheduler with a marker indicating that scheduling of the load microinstruction is to be deferred.

Column 12, lines 7-22 show that a PA buffer is used to detect stores that interfere or collide with loads. This section also shows that when a collision (a match by the PA buffer) is found and the corresponding operation is a load that is younger than a store, then a scheduler entry is defined that indicates the load is to be retried, that is the load is to not be executed (deferred) since it has a dependency on an older store for which the data is not available and will be retried later. Markers (figure 3, element 6, R and T) are used to convey that a load is to be retried and that a load is dependent on an older store as shown in column 11, lines 25-31.

18. In regard to claim 6, Keller discloses the scheduling method of claim 5, further comprising storing a scheduler entry identifier (figure 3, element 66, SID) of the older store with the load microinstruction. Column 11, lines 22-25 show that the SID field in the scheduler entries indicate the store (older store) operation interfered (collided) with.

19. In regard to claim 7, Keller discloses the scheduling method of claim 5, further comprising scheduling the load microinstruction for execution after the marker is cleared. Column 12, lines 44-46 show that scheduling of a load for execution (it is still placed in the scheduling buffer when not executed as shown above) is inhibited until after the store is scheduled for execution. This means that the load entry in the scheduler that has markers preventing execution, as discussed previously, will clear the markers so that execution proceeds.

20. In regard to claim 8, Keller discloses the scheduling method of claim 7, further comprising scheduling other instructions dependent upon the load microinstruction to execute after the load microinstruction executes. It is inherent that other instructions dependent on the load will execute after the load executes since they have not executed due to the dependency and must execute to keep the program flowing.

21. In regard to claim 9, Keller discloses the scheduling method of claim 5, further comprising deferring scheduling of other instructions dependent upon the load microinstruction when scheduling of the load microinstruction is deferred. It is inherent that if loads are deferred due to dependency on other unscheduled instructions that instructions with a dependency on the load, when deferred from scheduling, will also be deferred.

22. In regard to claim 13, Keller discloses an execution unit for a processing agent, comprising:

a. a scheduler (figure 1, element 36) operating according to the method of claim 5.

b. a register file (figure 1, element 38A);

c. and a plurality of execution modules (figure 1, elements 40A and 40B);

d. wherein the scheduler, the register file and the execution modules each are coupled to a common communication bus. Figure 1 shows that the scheduler, register files, and execution modules have a bus that begins at the scheduler, passes through the register file, and couples the execution modules together.

23. In regard to claim 14, Keller discloses a scheduling method, comprising:

a. predicting whether a new load microinstruction collides with a first previously received store microinstruction; Column 10, lines 35 – 55 show that a STLF (store to load forwarding, column 2, lines 14-27) predictor makes a prediction for each load instruction (new load) based on past executions whether it will interfere or collide with a store operation. Column 10, line 61 – column 11, line 8 shows that the embodiment of focus in the disclosure is where the store is older than the load.

b. when a collision is detected, storing the load microinstruction in a scheduler with a dependency pointer to a second previously received store microinstruction. Column 12, lines 7-22 show that a PA buffer is used to detect stores that interfere or collide with loads. This section also shows that when a collision (a match by the PA buffer) is found and the corresponding operation is a load that is younger than a store, then a scheduler entry is defined that indicates the load is to be retried, that is the load is to not be executed (deferred) since it

has a dependency on an older store for which the data is not available and will be retried later. Markers or pointers (figure 3, element 6, R and T) are used to convey that a load is to be retried and that a load is dependent on an older store as shown in column 11, lines 25-31. Since the terms first and second are merely names and may in fact name the same element, the examiner is taking the first and second microinstructions to be the same microinstruction.

24. In regard to claim 15, Keller discloses the scheduling method of claim 14, further comprising scheduling the load instruction for execution after the dependency pointer is cleared. Column 12, lines 44-46 show that scheduling of a load for execution (it is still placed in the scheduling buffer when not executed as shown above) is inhibited until after the store is scheduled for execution. This means that the load entry in the scheduler that has markers preventing execution, as discussed previously, will clear the markers so that execution proceeds.

25. In regard to claim 16, Keller discloses the scheduling method of claim 15, further comprising scheduling other instructions dependent upon the load microinstruction to execute after the load microinstruction executes. It is inherent that other instructions dependent on the load will execute after the load executes since they have not executed due to the dependency and must execute to keep the program flowing.

26. In regard to claim 17, Keller discloses the scheduling method of claim 14, further comprising deferring scheduling of other instructions dependent upon the load microinstruction when scheduling of the load microinstruction is deferred. It is inherent that if loads are deferred due to dependency on other unscheduled instructions that

instructions with a dependency on the load, when deferred from scheduling, will also be deferred.

27. In regard to claim 21, Keller discloses an execution unit for a processing agent, comprising:

a. a scheduler (figure 1, element 36) operating according to the method of claim 14;

b. a register file (figure 1, element 38A);

c. and a plurality of execution modules(figure 1, elements 40A and 40B);

d. wherein the scheduler, the register file and the execution modules each are coupled to a common communication bus. Figure 1 shows that the scheduler, register files, and execution modules have a bus that begins at the scheduler, passes through the register file, and couples the execution modules together.

28. In regard to claim 22, Keller discloses a dependency management method, comprising, upon execution of a STD uop:

a. comparing an identifier of the STD uop to dependency pointers of other uops stored by a scheduler; Column 12, lines 7-22 show that PA buffer entries (identifiers) are compared for store (STD as defined above in the claim objections) and load operations or microinstructions (uops).

b. and clearing any dependency pointers that match the identifier. Markers or pointers (figure 3, element 6, R and T) are used to convey that a load is to be retried and that a load is dependent on an older store as shown in column 11,

lines 25-31. Column 12, lines 44-46 show that scheduling of a load for execution (it is still placed in the scheduling buffer when not executed as shown above) is inhibited until after the store is scheduled for execution. This means that the load entry in the scheduler that has markers preventing execution will clear the markers so that execution proceeds.

29. In regard to claim 23, Keller discloses the dependency management method of claim 15, wherein the identifier represents a location in the scheduler where the STD uop is stored. Column 12, lines 7-22 and figure 3 show that each PA buffer entry (identifier) corresponds to a scheduler entry and thus represents a location in the scheduler that contains a uop.

30. In regard to claim 24, Keller discloses the dependency management method of claim 15, wherein the identifier represents a location in a store unit where data responsive to the STD uop is stored. Column 11, line 67 – column 12, line 1 show that a physical address (just as is stored in the PA buffer and thus the same identifier) is provided to the store queue for storage. Since the identifier (physical address) is in itself a location and is stored in this store unit, the claim is met.

Claim Rejections - 35 USC § 103

31. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

32. Claims 10-12 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller in view of Abramson (5,898,854) and Hennessy (Computer Organization and Design).

33. In regard to claim 10,

a. Keller discloses the scheduling method of claim 5,

b. Keller does not explicitly show wherein the store microinstruction is one of a plurality of microinstructions representing a store instruction, wherein a first microinstruction is to transfer data to a store unit and a second microinstruction is to calculate an address of the store instruction.

c. Abramson has taught in column 6, lines 12-15 that the store instruction is made up of store address (calculate address) and store data (transfer data) operations or microinstructions.

d. Hennessy has taught in the introduction to section 5.5 on pages 399-400 that microinstructions provide method of specifying control that makes understanding and design of a system easier since complex instructions are broken up into smaller and simpler operations. The ability to make system design and comprehension easier would have motivated one of ordinary skill in the art to use microinstructions to specify as many simple operations as possible, specifically the store address and store data microinstructions of Abramson. With this modification in place, the store microinstruction of Keller is broken up further into the store address and store data microinstructions of Abramson.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to use the store address and store data microinstructions for the store instructions so that system design and understanding is easier as taught by Hennessy.

34. In regard to claim 11, Keller in view of Abramson and Hennessy disclose the scheduling method of claim 10, further comprising clearing the marker of the load microinstruction after the first store microinstruction executes. Column 12, lines 44-46 show that scheduling of a load for execution (it is still placed in the scheduling buffer when not executed as shown above) is inhibited until after the store is scheduled for execution. This means that the load entry in the scheduler that has markers preventing execution, as discussed previously, will clear the markers once the store is completed and the dependency is removed so that execution proceeds.

35. In regard to claim 12, Keller in view of Abramson and Hennessy disclose the scheduling method of claim 10, wherein the prediction determines a collision between the load microinstruction and the second store microinstruction. As shown above in the sections cited, the dependency between the load and store instructions stems from the data not being ready and therefore the second microinstructions, which directs the transfer of data, is the microinstruction that a collision with the load is detected and predicted for.

36. In regard to claim 18,

a. Keller discloses the scheduling method of claim 5,

b. Keller does not explicitly show wherein the store microinstruction is one of a plurality of microinstructions representing a store instruction, wherein a first microinstruction is to transfer data to a store unit and a second microinstruction is to calculate an address of the store instruction.

c. Abramson has taught in column 6, lines 12-15 that the store instruction is made up of store address (calculate address) and store data (transfer data) operations or microinstructions.

d. Hennessy has taught in the introduction to section 5.5 on pages 399-400 that microinstructions provide method of specifying control that makes understanding and design of a system easier since complex instructions are broken up into smaller and simpler operations. The ability to make system design and comprehension easier would have motivated one of ordinary skill in the art to use microinstructions to specify as many simple operations as possible, specifically the store address and store data microinstructions of Abramson. With this modification in place, the store microinstruction of Keller is broken up further into the store address and store data microinstructions of Abramson.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to use the store address and store data microinstructions for the store instructions so that system design and understanding is easier as taught by Hennessy.

37. In regard to claim 19, Keller in view of Abramson and Hennessy disclose the scheduling method of claim 18, further comprising clearing the dependency pointer of

the load microinstruction after the first store microinstruction executes. Column 12, lines 44-46 show that scheduling of a load for execution (it is still placed in the scheduling buffer when not executed as shown above) is inhibited until after the store is scheduled for execution. This means that the load entry in the scheduler that has markers preventing execution, as discussed previously, will clear the markers once the store is completed and the dependency is removed so that execution proceeds.

38. In regard to claim 20, Keller in view of Abramson and Hennessy disclose the scheduling method of claim 18, wherein the prediction determines a collision between the load microinstruction and the second store microinstruction. As shown above in the sections cited, the dependency between the load and store instructions stems from the data not being ready and therefore the second microinstructions, which directs the transfer of data, is the microinstruction that a collision with the load is detected and predicted for

Conclusion

39. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have been cited to further show the art with respect to load/store collisions.

US Pat No 6,108,770 to Chrysos teaches scheduling loads and handling collisions including deferring the load.

US Pat No 5,691,920 to Levine shows scheduling loads including their type, operand pointers, and exception or collision information.

US Pat No 5,557,763 to Senter discloses buffers for holding load execution information including the operation type, collision information, valid information, and operand addresses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
June 10, 2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100